

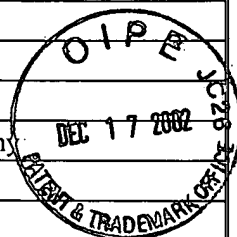
Substitute for Form 1449A/PTO (Modified)

# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

*(use as many sheets as necessary)*

**Complete if Known**

Application Number	09/831,539
Filing Date	04/15/2002
First Named Inventor:	Anand S. Murthy
Group Art Unit	2823
Examiner Name	Kebede, Brook
Attorney Docket Number	42390P6624US



Sheet

1

of

2

Attorney Docket Number

42390P6624US

## U.S. PATENT DOCUMENTS

[illegible]

## FOREIGN PATENT DOCUMENTS

[illegible]

Examiner  
Signature

Brook Kibell

#### Date Considered

3/8/2002

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<sup>1</sup>Unique citation designation number. <sup>2</sup>See attached Kinds of U.S. Patent Documents. <sup>3</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard S.3). <sup>4</sup>For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. <sup>5</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>6</sup>Applicant is to place a check mark here if English language Translation is attached.

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Sheet	2	of	2		
<b>OTHER ART - NO PATENT LITERATURE DOCUMENTS</b>					
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T <sup>2</sup>
BK		MITANI, Y., ET AL., Buried Source and Drain (BSD) Structure for Ultra-shallow Junction Using Selective Deposition of Highly Doped Amorphous Silicon, 1996 Symposium on VLSI Technology, Digest of Technical Papers, Honolulu, The IEEE Electron Devices Society, The Japan Society of Applied Physics, IEEE CAT No. 96CH35944, JSAP CAT. No. AP961207, ©1996 IEEE, pages 176-177.			
BK		NAKAHARA, Y., ET AL., Ultra-shallow in-situ-doped raised source/drain structure for sub-tenth micron CMOS, 1996 Symposium on VLSI Technology Digest of Technical Papers, ©1996 IEEE, pages 174-175.			
BK		UCHINO, TAKASHI, ET AL., A Raised Source/Drain Technology Using In-situ P-doped SiGe and B-doped Si for 0.1-µm CMOS ULSIs, ©1997 IEEE, pgs. 479-482.			
BK		WOLF, S. AND TAUBER, R.N., for the VLSI Era, Volume 1 - Process Technology, pages 173-174 and pages 545-547.			
BK		Search Report for PCT/US99/26224, mailed February 10, 2000, 5 pages.			
BK		Written Opinion for PCT/US99/26224, mailed October 30, 2000, 4 pages.			

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